REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 2-17 are pending in the present application. No claims are amended, canceled or added by the present amendment.

In the outstanding Office Action, Claims 2-4, 6, 13 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Akiyama et al. (herein "Akiyama") in view of U.S. Publication No. 2001/0040255 to Tanaka; Claims 5 and 14 were rejected under 35 U.S.C. § 103(a) as unpatentable over Akiyama in view of Tanaka and U.S. Patent No. 6,798,040 to Reznik; and Claims 1-3, 6 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Tanaka.

Applicants and Applicants' representative gratefully acknowledge the Examiner's comments in the Response to Arguments portion of the Office Action, which includes comments and questions regarding the Amendment filed February 6, 2006. Responses to those questions are believed to be addressed in the following discussion. However, if additional questions are raised by the following discussion or if previously raised questions are not adequately addressed, the Examiner is kindly requested to contact Applicants' representative at the telephone number below.

First, Applicants respectfully traverse the rejection of Claims 1-4 and 6 under 35 U.S.C. § 103(a) as unpatentable over Akiyama and Tanaka.

Amended Claim 2 is directed to an insulated gate bipolar transistor including, in part, a semiconductor substrate including first and second main surfaces, and first and second semiconductor layers of first and second conductivity types, respectively, formed on the second main surface. A distance between i) the first main surface and ii) an interface

between an electrode and each of the first and second semiconductor layers is equal to 200 μm or smaller. Independent Claim 3 includes similar features.

In a non-limiting example, Applicants' Figure 2 shows an integrated gate bipolar transistor including an n^--type semiconductor substrate 1 having a first main surface 1S1 and first and second semiconductor layers 8 and 9 formed on a second main surface 1S2. A second electrode 10 is formed on the first and second semiconductor layers 8 and 9, with an interface IF between the semiconductor layers and the electrode. A thickness D of the wafer measured from the interface IF to the first main surface 1S1 is equal to 200 μm or smaller.

As discovered by the Applicants, the wafer should advantageously be 200 μm or smaller in an IGBT with a built-in freewheeling diode to avoid undesirable increases in Vf and VCE(sat) as shown in Applicants' Figures 4-8, and as described in the specification at page 18, line 5, to page 19, line 6. For example, Applicants' Figure 4A shows that VCE(sat) increases dramatically for values of wafer thickness greater than 200 μm.

Applicants respectfully submit that none of the references in the Office Action, whether taken individually or in combination, teach or suggest a wafer thickness of 200 μm or less.

First, Applicants note that substrate thickness is not mentioned at all by Tanaka. Further, Akiyama merely indicates that a device has a structure including an alternating N/P type impurity region doped in a substrate to a depth of 30 μm. Akiyama also indicates that a thickness of the remaining portion of the substrate, including a N^- type region, and N^+ and P^+ IGBT regions is 190 μm. Although Akiyama does not describe the fabrication process used to make this device, it would have been clear to one of skill in the art of semiconductor device fabrication that regardless of whether this device was made by impurity diffusion or ion implantation, the initial wafer thickness would be 220 μm. That is because, as known in the art, process steps that change an impurity concentration in a substrate, such as diffusion or

implantation, do not substantially change or increase a thickness of the wafer. Instead, such process steps change a concentration of an impurity within a region that is inside the existing semiconductor wafer. In other words, impurity regions, such as the N/P regions shown in Akiyama's Fig. 1a, are not attached to a substrate. Instead, such impurity regions are formed within an existing substrate by adding impurities to existing portions of a substrate.

Accordingly, it would have been clear to one of skill in the art that a process of making the semiconductor device described by Akiyama would begin with a wafer having a thickness of 220 μm, into which N and P type impurities might be added (e.g., by diffusion or implantation) such that the impurities reach into the substrate at a depth of 30 μm. Further, although Akiyama indicates that the 220 μm wafer shown in Fig. 1a includes a 190 μm thick remaining portion including the N^- type region and the IGBT regions, as well as a 30 μm thick N/P region, Akiyama is silent regarding any advantages for selecting those region thicknesses, and does not teach or suggest any device properties related to those region thicknesses. In addition, Akiyama only describes a wafer having a thickness of 220 μm and does not describe or otherwise suggest any other wafer having a different thickness or suggest any step or motivation for reducing a thickness of a wafer.

As noted above, Tanaka is completely silent regarding a thickness of a wafer, and in FIGs. 10 and 11, Tanaka illustrates a device having N/P regions 12 and 2B that are implanted into an existing semiconductor substrate 1 up to a depth of 0.8 μm.[1] Further, Tanaka does not describe the thickness of semiconductor substrate 1 or indicate any reason to reduce the substrate thickness.

Applicants respectfully traverse the assertion in the Office Action that

> it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Akiyama by using a thickness of less than 1 micron for the first and second semiconductor regions as taught by Tanaka . . . Furthermore, when the thickness of the first and second

[1] Tanaka at page 10, paragraph [0187].

> semiconductor regions as taught by Tanaka is incorporated into the device of Akiyama, the distance between said first main surface and said interface is 200 microns or smaller (190 microns + 0.8 microns).[2]

First, Applicants note that if one were to combine the teachings of Tanaka and Akiyama, without adding additional steps that are not taught or suggested in the references, one would not obtain the claimed invention. As described above, Akiyama only describes a wafer thickness of 220 μm and an N/P impurity depth of 30 μm. Further, Applicants respectfully point out that changing a first wafer thickness to a second, smaller wafer thickness, requires additional process steps, not fewer process steps. For example, extra polishing or etching steps would be required to remove wafer material and reduce a thickness of a wafer from 220 μm to 200 μm. The references in the Office Action are silent regarding any such process steps or any motivation to perform such extra steps. Therefore, although there is no motivation to do so, if one of skill in the art were to combine the teachings of Tanaka with Akiyama, one would implant N/P regions to a depth of 0.8 μm within an existing 220 μm substrate. Akiyama does not teach or suggest any other wafer thickness.

As noted in the specification and as described above, Applicants discovered specific advantages that may be achieved by maintaining a wafer thickness of 200 μm or smaller. However, Tanaka and Akiyama are silent regarding those advantages, and do not describe any wafer having a thickness of 200 μm or smaller. For one to obtain a wafer thickness of 200 μm or smaller starting with the 220 μm described by Akiyama, one would have to perform additional steps, such as etching or polishing, to remove wafer material, and such steps, or even motivation to perform such steps, are absent from the applied references.

Further, Applicants respectfully note that one of skill in the art would not assemble a semiconductor device by starting with a 190 μm semiconductor substrate and adding a 0.8 μm N/P impurity region to obtain a wafer having a thickness of 190.8 μm, as suggested in the

[2] Office Action at page 4, lines 8-10 and 13-16.

Office Action.[3] As discussed above, one of skill in the art would have known that impurity regions are added to existing semiconductor substrates by diffusion or implantation, without substantially increasing the wafer thickness. Thus, to obtain a wafer with a 190 μm region (i.e., including the N^- region and the IGBT region) and a 0.8 μm N/P impurity region, as proposed by the Office Action, one of skill in the art would start with a wafer having a thickness of 190.8 μm, and Applicants respectfully submit that the references in the Office Action do not teach or suggest any wafer having that thickness. Further, there is no motivation or reason mentioned in the applied references for performing any additional steps to reduce a thickness of a wafer or to use a different wafer thickness other than the 220 μm thick wafer described in Akiyama.

Further, Applicants respectfully traverse the assertion in the Office Action that "Applicant has suggested an additional modification to Akiyama, where the thickness of the N- region is increased from 190 μm to 220 μm."[4] However, as noted above, Akiyama does not teach or suggest an N- region having a particular thickness. Instead, Akiyama shows a depth of impurities in the N/P region, and shows a total dimension of the remaining portions of the wafer, including the N^- region and the N^+ and P^+ IGBT regions. Accordingly, Applicants have suggested no modification to a thickness of an N- region in Akiyama at least because there is no teaching of an N^- region thickness in Akiyama or Tanaka.

Further, Akiyama does not teach or suggest fabricating a device by starting with a 190 μm N- substrate/IGBT region and adding to that an additional 30 μm N/P region, because as one of skill in the art knows, impurity regions are not added or attached to each other. Instead, one of skill in the art would have known that impurities are added within an existing substrate to create an impurity region within the existing substrate. Thus, contrary to the

[3] Office Action at page 4, line 13-16.
[4] Office Action at page 8, lines 18-19.

assertion in the Office Action,[5] Applicants do not suggest that one of skill in the art would take steps to ***increase*** an N- region if Akiyama and Tanaka were combined. On the other hand, Applicants point out that a change in the dimensions of thickness of a remaining portion of a wafer (as measured by Akiyama) would be the normal and expected outcome if one of skill in the art were to combine the teachings of Akiyama and Tanaka, that is if the artisan were to insert an impurity region having a depth of 1 μm or less (i.e., the depth taught by Tanaka) within a 220 μm semiconductor substrate (i.e., the wafer thickness taught by Akiyama).

Further, Applicants point out that Akiyama does not teach or suggest a N^- region plus IGBT portion that exists independent of the wafer or independent of other layers in the wafer, or a N^- region that other layers can be added on top of or beneath. Instead, Akiyama merely shows an example of a 220 μm thick wafer having a 30 μm thick N/P impurity layer, which leaves 190 μm for everything else (e.g., for the N^- impurity layer, the IGBT P^+ base layer and N^+ layer). If an artisan were to change the depth of the N/P impurity layer from 30 μm to 1 μm, as suggested by Tanaka, the artisan would obtain a 220 μm thick wafer having a 1 μm thick N/P impurity layer, with 219 μm left for everything else.

Accordingly, Applicants respectfully submit that Akiyama and Tanaka do not teach or suggest "a distance between said first main surface and said interface is equal to 200 μm or smaller," as recited in independent Claims 2 and 3.

Therefore, Applicants respectfully submit that independent Claims 2 and 3, and claims depending therefrom, patentably define over Akiyama and Tanaka, whether taken individually or in combination.

Accordingly, Applicants respectfully request the rejection of Claims under 35 U.S.C. § 103(a) as unpatentable over Akiyama and Tanaka be withdrawn.

[5] Office Action at page 8, lines 18-19.

Further, Applicants respectfully traverse the rejection of Claims 5 and 14 under 35 U.S.C. § 103(a) as unpatentable over Akiyama in view of Tanaka and Reznik. Claims 5 and 14 depend from Claims 2 and 3, which as discussed above are believed to patentably define over Akiyama and Tanaka. Further, Reznik does not teach or suggest the claimed features lacking in the disclosures of Akiyama and Tanaka. Accordingly, it is respectfully requested that rejection also be withdrawn.

In addition, Applicants respectfully traverse the rejection of Claims 1-3, 6 and 15 under 35 U.S.C. § 103(a) as unpatentable over Tanaka.

First, as discussed above, independent Claims 2 and 3, and claims depending therefrom, are believed to patentably define over Tanaka. Moreover, Claim 1 was previously canceled. In addition, Applicants respectfully traverse the assertion in the Office Action that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a distance between the first surface and the interface equal to or less than 200 microns, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art."[6] The Applicants discovered the importance of controlling the wafer thickness, and as discussed above, Tanaka is silent regarding a thickness of a wafer. Tanaka does not teach or suggest that a thickness of a wafer is even a relevant consideration. Thus, it is clear that Tanaka does not indicate or suggest that the thickness of a wafer is a "result effective variable." Applicants respectfully submit that finding motivation in Tanaka to vary a thickness of a wafer is impermissible hindsight reasoning.

Accordingly, Applicants respectfully request the rejection of claims as unpatentable over Tanaka under 35 U.S.C. § 103(a) also be withdrawn.

[6] Office Action at page 7, lines 7-11.

Accordingly, Applicants respectfully submit that independent Claims 2 and 3, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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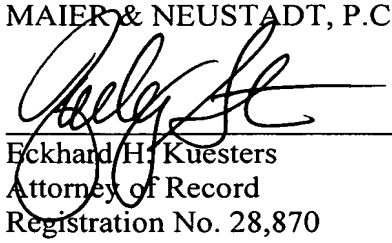

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